

Computer Organisation (ID) (IT 3001)

Course Code	(ID) IT-3001	Credits-4	L-3, T-1, P-0
Name of the Course	Computer Organisation		
Lectures to be Delivered	52 (1 Hr Each) (L= 39, T = 13 for each semester)		
Semester End Examination	Max. Marks: 100	Min. Pass Marks: 40	Maximum Time:3hrs
Continuous Assessment (based on sessional tests (2) 50%, Tutorials/Assignments 30%, Quiz/Seminar 10%, Attendance 10%)			Max. Marks: 50

Instructions

- For Paper Setters:** The question paper will consist of five sections A, B, C, D, and E. Section E will be Compulsory, it will consist of a single question with 10-20 subparts of short answer type, which will cover the entire syllabus and will carry 40% of the total marks of the semester end examination for the course. Section A, B, C and D will have two questions from the respective sections of the syllabus and each question will carry 15% of the total marks of the semester end examination for the course.
- For Candidates:** Candidates are required to attempt five questions in all selecting one question from each of the sections A, B, C and D of the question paper and all the subparts of the questions in section E.. Use of non-programmable calculators is allowed.

Section A

Basics: An introduction to computers with block diagrams, Computers generations, Impact of technology.
Logic Design Techniques: Designing Combinations logic using Karnaugh maps with building blocks of basic gates, Multiplexers, de-multiplexers, decoders, encoders, arithmetic/logic unit.

Instruction codes, Computers registers and instructions, timing, and control, Instructions cycle, memory reference instruction, I-O interruption,

Basic sequential logic blocks of flip-flops, registers, shift registers and counters, Finite state Machine using state tables.

Section B

Computer Arithmetic- Adder, and Subtractor circuits, Booth Multiplication Algorithm, Performance bench marks.

Control Path Design: Sequence counter method, Micro programmed controllers address sequencing, symbolic micro-instructions.

Section C

Central Processing Unit: Registers General register origination, stack organization, instructions formats, address instructions, addressing modes, data transfer and manipulations, program control, RISC instruction set design, three address instructions and arithmetic pipelines with example of floating point adder, instructions pipelines, advanced pipelining using instruction level parallelism.

Section D

Memory origination: Memory device characteristics, random access memory, serial access memory, virtual memory, associative memory, cache memory, memory management hardware.

I/O Organization: I/O interface asynchronous data transfer, DMA interrupt, I/O processor.

Books:

1. M. Morris Mano ,Computer system & Architecture PHI
2. Hayes .J.P ,Computer architecture and organisation ,
3. M.Morris and Charles R. Kinre , Logic and computer design Fundamentals –. PHI 1995