

Computer Architecture (ID) (IT – 4001)

Course Code	(ID) IT-4001	Credits-4	L – 3, T-1, P-0
Name of the Course	Computer Architecture		
Lectures to be Delivered	52 (1 Hr Each) (L= 39, T = 13 for each semester)		
Semester End Examination	<i>Max. Marks: 100</i>	<i>Min. Pass Marks: 40</i>	Maximum Time:3hrs
Continuous Assessment (based on sessional tests (2) 50%, Tutorials/Assignments 30%, Quiz/Seminar 10%, Attendance 10%)			<i>Max. Marks: 50</i>

Instructions

1. **For Paper Setters:** The question paper will consist of five sections A, B, C, D, and E. Section E will be Compulsory, it will consist of a single question with 10-20 subparts of short answer type, which will cover the entire syllabus and will carry 40% of the total marks of the semester end examination for the course. Section A, B, C and D will have two questions from the respective sections of the syllabus and each section will carry 15% of the total marks of the semester end examination for the course
2. **For Candidates:** Candidates are required to attempt five questions in all selecting one question from each of the sections A, B, C and D of the question paper and all the subparts of the questions in section E. Use of non-programmable calculators is allowed.

Section – A

Fundamentals of Computer Design: Introduction, Measuring and Reporting Performance, Quantitative principles of Computer Design, The Concept of Memory Hierarchy

Instruction Set Principles and Examples: Classifying Instruction Set Architectures; Memory Addressing; Operations in the Instruction Set, Type and Size of Operands, Encoding an instruction set, The DLX Architecture

Section – B

Pipelining: What is Pipelining? The Basic Pipeline for DLX, the major hurdle of pipelining-pipeline hazards, What Makes pipelining hard to implement? The MIPS R4000 pipeline

Advanced Pipelining and Instruction-Level Parallelism: Instruction-level parallelism: Concepts and Challenges, Overcoming Data Hazards with Dynamic Scheduling, Reducing Branch Penalties with Dynamic Hardware prediction, Taking advantage of more ILP with multiple issue, Compiler Support for Exploiting ILP

Section – C

Memory-Hierarchy Design: Introduction, The concept of Cache memory, Reducing Cache misses, Reducing Cache miss Penalty, Reducing Hit Time Main Memory, Virtual Memory, and memory protection.

Storage systems: Types of Storage devices, Buses-Connecting I/O Devices to CPU/Memory, I/O Performance Measures, Reliability, Availability and RAID, UNIX File system performance.

Section – D

Interconnection Networks: A simple network, connecting the interconnection network to the computer, interconnection network media, connecting more than two computers, practical issues for commercial interconnection networks, examples of interconnection networks.

Multiprocessors: Characteristics of Application Domains, Centralized Shared Memory Architectures, Distributed Shared- Memory Architectures, Synchronization.

BOOKS

1. Computer Architecture A Quantitative Approach, John L. Hennessy & David A. Patterson, 2nd Edition, Harcourt Asia Pte. Ltd., 1996.
2. Computer Architecture & Organisation, McGraw Hill, 3rd Edition, John Hayes, 1998.

3. Computer System Architecture PHI, 3rd edition, M. Morris Mano.
4. Computer Architecture and Parallel Processing, McGraw Hill Book Company, Hwang and Briggs.
5. Advanced Computer Architecture: Parallelism, Scalability, Programmability, Kai Hwang, McHill, Inc., 1993.